CLAIMS

What is claimed is:

1. A switchable low pass filter comprising:

a first switch connected to a first resistive element;

a second switch connected to a second resistive element;

a capacitive element connected to said first resistive element and said second resistive element; and

a controller connected to said first switch and said second switch, said controller operative to open and close at least one of said first switch and said second switch.

2. A switchable low pass filter according to claim 1, wherein said first resistive element has a resistance which is smaller than the resistance of said second resistive element.

3. A device comprising:

a plurality of resistive elements;

at least one switch connected to one of said resistive elements;

a capacitive element connected to said resistive elements thereby forming a low pass filter with said resistive elements; and

a controller connected to said at least one switch, said controller operative to open and close said at least one switch thereby switching the resistance of said low pass filter.

4. A device comprising:

a plurality of resistive elements;

at least one switch connected to one of said resistive elements;

a capacitive element connected to said resistive elements thereby forming a low pass filter with said resistive elements, said low pass filter having a response time; and

a controller connected to said at least one switch, said controller operative to open and close said at least one switch thereby changing said response time.

5. A digital to analog converter comprising:

a digital circuit which produces a pulse modulated signal; and

a switchable low pass filter having a plurality of response times for converting said pulse modulated signal to an analog signal having ripples,

wherein switching said low pass filter among said response times changes the size of said ripples.

6. A digital to analog converter according to claim 5, wherein said digital circuit is a pulse width modulation circuit.

7. A digital to analog converter according to claim 5, wherein said digital circuit is a pulse density modulation circuit.

8. A digital to analog converter according to claim 5, wherein said switchable low filter comprises:

a first switch connected to a first resistive element;

a second switch connected to a second resistive element;

a capacitive element connected to said first resistive element and said second resistive element; and

a controller connected to said first switch and said second switch, said controller operative to open and close at least one of said first switch and said second switch.

9. A digital to analog converter according to claim 8, wherein said first resistive element has a resistance which is smaller than the resistance of said second resistive element.

10. A device for producing a pulse density modulated signal whose pulse timing is jittered, the device comprising:

a flip flop for storing a value;

a random number generator for producing a substantially random number; and

an adder for adding said substantially random number and a multi-bit number to said value, said adder having an upper limit,

wherein a pulse is produced when the sum of said substantially random number, said multi-bit number and said value is not less than said upper limit.

11. A method for producing a pulse density modulated signal whose pulse timing is jittered, the method comprising the steps of:

adding a substantially random number and a multi-bit number to a value stored in a flip flop, thereby producing a sum;

if said sum is less than an upper limit, storing said sum in said flip flop, thereby replacing said value;

if said sum is not less than said upper limit,

producing a pulse;

subtracting said upper limit from said sum, thereby producing a result; and

storing said result in a flip flop; and

repeating said steps.

SUMMARY OF THE INVENTION

There is provided in accordance with a preferred embodiment of the present invention a switchable low pass filter including a first switch connected to a first resistive element, a second switch connected to a second resistive element, and a capacitive element connected to the first and second resistive elements. The switchable low pass filter also includes a controller connected to the first switch and the second switch, the controller operative to open and close at least one of the first switch and the second switch.

Moreover, in accordance with a preferred embodiment of the present invention, the first resistive element has a resistance which is smaller than the resistance of the second resistive element.

There is also provided in accordance with a preferred embodiment of the present invention a device including a plurality of resistive elements, at least one switch connected to one of the resistive elements, and a capacitive element connected to the resistive elements. The capacitive element forms a low pass filter with the resistive elements. The device also includes a controller connected to the at least one switch, the controller operative to open and close the at least one switch thereby switching the resistance of the low pass filter.

There is also provided in accordance with a preferred embodiment of the present invention a device including a plurality of resistive elements, at least one switch connected to one of the resistive elements, and a capacitive element connected to the resistive elements. The capacitive element forms a low pass filter with the resistive elements, and the low pass filter has a response time. The device also includes a controller connected to the at least

one switch, the controller operative to open and close the at least one switch thereby changing the response time.

There is also provided in accordance with a preferred embodiment of the present invention a digital to analog converter. The digital to analog converter includes a digital circuit which produces a pulse modulated signal, and a switchable low pass filter having a plurality of response times for converting the pulse modulated signal to an analog signal having ripples. Switching the low pass filter among the response times changes the size of the ripples.

Moreover, in accordance with a preferred embodiment of the present invention, the digital circuit is a pulse width modulation circuit or a pulse density modulation circuit.

Furthermore, in accordance with a preferred embodiment of the present invention, the switchable low filter includes a first switch connected to a first resistive element, a second switch connected to a second resistive element, and a capacitive element connected to the first and second resistive elements. The switchable low pass filter also includes a controller connected to the first switch and the second switch, the controller operative to open and close at least one of the first switch and the second switch.

Additionally, in accordance with a preferred embodiment of the present invention, the first resistive element has a resistance which is smaller than the resistance of the second resistive element.

There is also provided in accordance with a preferred embodiment of the present invention a device for producing a pulse density modulated signal whose pulse timing is jittered. The device includes a flip flop for storing a value,

a random number generator for producing a substantially random number, and an adder. The adder adds the substantially random number and a multi-bit number to the value. The adder has an upper limit. A pulse is produced when the sum of the substantially random number, the multi-bit number and the value exceeds the upper limit.

There is also provided in accordance with a preferred embodiment of the present invention a method for producing a pulse density modulated signal whose pulse timing is jittered. The method includes the following steps: adding a substantially random number and a multi-bit number to a value stored in a flip flop, thereby producing a sum; if the sum is less than an upper limit, storing the sum in the flip flop, thereby replacing the value; if the sum is not less than the upper limit, producing a pulse, subtracting the upper limit from the sum, thereby producing a result, and storing the result in a flip flop; and repeating the steps.